REMARKS

The claims are claims 1, 3, 9, 10 and 18 to 20.

Claims 1, 10, 19 and 20 have been amended to further clarify the subject matter.

Claims 1, 9, 10, 12, and 18 to 20 were rejected under 35 U.S.C. 102(e) as anticipated by Hansen et al U.S. Published Patent Application No. 2003/0110197 A1.

Claims 1, 10, 19 and 20 recite subject matter not anticipated by Hansen et al. Claims 1, 10, 19 and 20 each recite critical paths and that first cells include critical paths and second cells do not. Claims 1 and 19 each recite that "said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than said longest amount of time." Claims 10 and 20 include similar recitations relative to a parallel multiplier core. Hansen et al includes no teaching regarding such critical paths. Accordingly, claims 1, 10, 19 and 20 are allowable over Hansen et al.

Claims 1, 10, 19 and 20 recite further subject matter not anticipated by Hansen et al. Claims 1 and 10 recite first and second cells that are "structurally the same." Claims 1 and 10 recite that "a width of at least one of said first plurality of transistors" forming the first cells "is greater than a width of a corresponding one of said second plurality of transistors" forming the corresponding second cells. Claims 19 and 20 recite that the

first Wallace tree cells are structurally the same as the second Wallace tree cells and that the first Booth decoder cells are structurally the same as the second Booth decoder cells. Claims 19 and 20 each recite that the first plurality of transistors of the first cells are a first width and that the corresponding second plurality of transistors of the corresponding second cells are a second smaller width. Thus claims 1, 10, 19 and 20 each recite cells that are structurally the same with differing transistor widths dependent upon whether the cell is within a critical path. Hansen et al neither teaches the width of a transistor difference nor teaches cells differing in any way dependent upon whether they are in a critical path. Therefore Hansen cannot anticipate this limitation of claims 1 and 10.

The OFFICE ACTION states in the Response to Arguments at page 5, line 12 to page 6, line 2:

> "The examiner respectfully submits that the rejection clearly addresses above under U.S.C. 102. To address further, the current language does not define clearly "the predetermined time" so the predetermined time can be any small arbitrary number which would meet the limitation cited in the claim. Further as clearly mentioned in the previous Office action, since the claims do not defined particularly the important of difference width of transistor nor they defined the exact relationship of the first and second plurality of transistors respectively, then if any transistor differs in width it would meet the limitation cited in the claim. Thus as reason by the examiner, it is impossible to manufacture all the transistors with exact the same width, then at least one of transistors would have difference width."

While the Examiner is correct that the predetermined time can be chosen arbitrarily small and that "it is impossible to manufacture all transistors with the same width," these arguments fail to take into account that the "predetermined time" limitation and the first and second width limitations are tied together in this invention. Claims 1 and 10 recite first transistors having the first width in

Wallace tree cells or Booth decoder cells in a critical path as defined by the predetermined time. Claims 1 and 10 also recite second transistors having the second width in Wallace tree cells or Booth decoder cells "not disposed on any of said at least one critical path." Thus the wider transistors are in a critical path and the narrower transistors cannot be in a critical path. Method claims 19 and 20 include similar limitations.

The OFFICE ACTION (even including the Response to Arguments) fails to point out where Hansen et al teaches this particularly claimed relationship between the predetermined time and the transistor width. The recited predetermined time divides the critical paths from non-critical paths. As recited in the claims, critical paths are always longer in time than non-critical paths. The claims also require that the second transistors in the non-critical paths be no wider than and optionally narrower than the first transistors in the critical paths. This is according to the teachings in paragraph [0008], [0009], [0031] to [0037]. In accordance with the teachings in the application, the critical paths would use the wider transistors which are faster but use more power. The non-critical paths would use the narrower transistors which are slower but use less power. In aggregate, this would make the circuit faster and use less power than using same sized transistors in all paths. Hansen et al fails to teach this relationship between the predetermined time defining which paths are critical and which are non-critical and the transistor widths. Accordingly, claims 1, 10, 19 and 20 are allowable over Hansen et al.

Claims 9 and 18 recite subject matter not anticipated by Hansen et al. Claims 9 and 18 recite "said at least one second cell is a most significant bit or a least significant bit and said at least one first cell is not a most significant bit or a least significant bit." Respective base claims 1 and 10 recite that

first cells include a critical path and second cells do not. Hansen et al includes no teaching regarding critical paths and no teaching that most significant bits or least significant bits are not a critical path (second cells) and that paths not the most significant bits nor the least significant bits are the critical path (first cells). While Hansen inherently includes most significant bit cells and least significant bit cells, Hanson fails to teach such cells are constructed with the different widths recited in respective base claims 1 and 10. Accordingly, claims 9 and 18 are allowable over Hansen et al.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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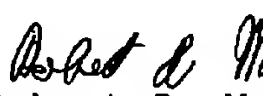
Respectfully submitted,



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